

REMARKS/ARGUMENTS

The preamble of claim 11 has been amended to overcome the 35 U.S.C. §101 rejection. Accordingly, it is respectfully submitted that pending claims 11-20 overcome the §101 rejection.

Pending claims 1, 11 and 21 stand rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,754,732 (Dixon). Applicant respectfully traverses the rejection. As to claim 1, Dixon nowhere teaches successively transferring data from a plurality of linked buffers in a first processor system to a plurality of linked buffers in a second processor system. In this regard, Dixon nowhere teaches a plurality of linked buffers from/to which data is transferred. Instead, Dixon only teaches a single transmit circular buffer and a single receive circular buffer. Thus Dixon further nowhere teaches successive transfer of data in (non-existent) multiple linked buffers from a transmitting side to such buffers on a receiving side. Nor does Dixon teach that these buffers are in different processor systems. Accordingly, for at least these reasons, claim 1 is patentable. For similar reasons, claims 11 and 21 are also patentable.

Pending claims 2, 3, 12, 13, 22 and 23 stand rejected under 35 U.S.C. §103(a) over Dixon in view of Deitel. Applicant respectfully traverses the rejection, at least for the same reasons discussed above regarding claim 1. Claim 2 is further patentable as the proposed combination nowhere teaches or suggests successive transfer of data. In this regard, Dixon (as discussed above) nowhere teaches or suggests such successive transfer. Nor does Deitel, which instead merely teaches that a linked list includes nodes each having a pointer to a next node. As to claim 3, neither reference teaches or suggests that a linked list is provided with descriptors to indicate the status of the buffers. In this regard, Deitel merely teaches that a linked list includes pointers to other nodes of the list. This is not a status of a buffer. Further, the Office Action concedes that Dixon nowhere teaches linked lists whatsoever. Final Office Action, p. 4. Thus neither reference teaches or suggests providing a linked list with descriptors to indicate status of buffers. For at least these reason, the above-listed dependent claims are further patentable.

Pending claims 4, 14, and 24 stand rejected under 35 U.S.C. §103(a) over Dixon in view of Deitel and further in view of U.S. Patent No. 5,568,443 (Dixon – ‘443). Applicant respectfully traverses the rejection, at least for the same reasons discussed above regarding claim 3. Claim 4 is further patentable as none of these references anywhere teach or suggest providing flags in descriptors to indicate whether a corresponding buffer is empty or full. Instead, Dixon – ‘443 merely teaches that a separate flags block is used to indicate the status of a FIFO buffer.

Nor is there any basis to combine Dixon – ‘443 with the other references, as Dixon – ‘443 is directed to a memory array, and has no bearing on the DMA system of Dixon. Thus the above-listed claims are further patentable.

Pending claims 5, 6, 9, 10, 15, 16, 19, 20, 25, 26, 29, 30, 32, 34 and 36 stand rejected under 35 U.S.C. § 103(a) over Dixon in view of U.S. Patent No. 6,412,029 (Mecklai). Applicant respectfully traverses the rejection. This rejection is improper at least for the same reasons discussed above regarding claim 1. That is, neither reference anywhere teaches or suggests successive data transfer between multiple linked buffers on both a transmitting side and a receiving side. These dependent claims are further patentable as the Office Action has failed to provide any valid motivation to combine the references. That is, the Office Action fails to provide any teaching or suggestion in either reference of the manner in which the enhanced DMA features of Dixon (which are only directed to updating queue directories upon a DMA transfer) are to be combined with the system of Mecklai. The mere statement that “one of ordinary skill in the art would have been motivated to make such combination to utilize the enhanced DMA features of Dixon within the cellular telephone” (Office Action, p. 7) utterly fails to provide any legally proper motivation to combine the references. *In re Lee*, 61 U.S.P.Q.2d 1430, 1435 (Fed. Cir. 2001). Thus it appears that the Office Action has engaged in a hindsight-based obviousness analysis disapproved by the Federal Circuit. To prevent such a hindsight-based analysis, the Federal Circuit requires that “to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant”. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1316-1317 (Fed. Cir. 2000). No such showing is present here. For this further reason, the above dependent claims are patentable.

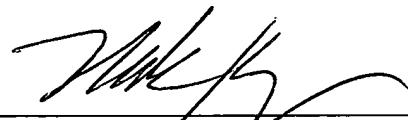
Dependent claim 9 is further patentable as neither of the references anywhere teach or suggest generating an interrupt when a linked buffer is empty based on a flag associated with a descriptor for the linked buffer. This is so, at least because neither of the references teach or suggest a descriptor associated with the buffer, nor such a descriptor having a flag associated therewith to indicate status of the buffer. Instead, Mecklai merely teaches that the buffer itself issues an interrupt when it is full. Mecklai, col. 5, lns. 5-10. For this further reason, claims 9, 10, 19, 20 and 29-30 are patentable.

Note further with respect to claims 32, 34 and 36 neither Dixon nor Mecklai anywhere teaches or suggests transfer of data from multiple linked buffers via FIFO buffers of first and second processor systems. For this further reason, these dependent claims are further patentable.

The rejection of claims 31, 33 and 35 under 35 U.S.C. §103 over Dixon in view of Valvano is overcome at least for same reasons discussed above regarding claim 1.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,



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